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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,431	02/06/2004	Mitsuharu Tai	NITT.0188	8944
7590	03/08/2006		EXAMINER	
Stanley P. Fisher Reed Smith LLP 3110 Fairview Park Drive, Suite 1400 Falls Church, VA 22042-4503				VU, PHU
			ART UNIT	PAPER NUMBER
			2871	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/772,431	TAI ET AL.	
	Examiner	Art Unit	
	Phu Vu	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-12 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_ is/are allowed.
- 6) Claim(s) 1-12 is/are rejected.
- 7) Claim(s) \_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_.

## DETAILED ACTION

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 1-4 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi et al US 6512504.**

**Regarding claims 1-4,** Yamauchi discloses an image display device provided with an active-matrix substrate comprising: an insulating substrate (fig. 1 element 11); and a plurality of circuit regions fabricated on said insulating substrate and including at least a pixel section and a pixel driving circuit section each of said pixel section and said pixel-driving circuit section having a polycrystalline silicon semiconductor film, wherein at least one of said plurality of circuit regions has a first type of a thin film transistor (fig. 2B 201) and a second type of a thin film transistor (fig. 2A), and an angular orientation of current flowing through a channel of said first type of a thin film transistor is nonparallel with an angular orientation of a direction of current flowing through a channel of the second type thin film transistor. Fig. 2B does not show the currents having different angular orientations however from fig. 2A it can be seen that the source

to drain of the respective TFTs are perpendicular (see fig. 2A elements 31 and 32 and 13 and 14). Regarding claims 2 considering all the TFTs corresponding to 201 to comprise the first circuit region and the second TFTs corresponding to 202 for each pixel comprise the second circuit region than the limitations of claim 2 are met. Regarding claims 3 and 4, the interpreting a "first-type circuit region" to correspond a part of the TFTs in the "first circuit region" and a "second-type circuit region" to correspond to a region including the TFTs all other TFTs of the "first circuit region" and "second circuit region" than these limitations are met.

**Regarding claim 8,** the limitation TFTs having "plural kinds of structures" according to the broadest reasonable interpretation can include having a TFT having a source gate and drain electrodes as the plural structures, which is met by any TFT.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi in view of Suzuki 6512247 in view of Takemura 6335555 in view of Ogawa US Patent No. 6479837 and further in view of Shinigawa et al 20030160239.**

**Regarding claims 5-6,** Suzuki teaches polycrystalline silicon films in a channel source and drain region constituting TFTs having an average crystalline diameter is 1

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micron or smaller (see column 2 lines 35-47) that do not require performance (column 4 lines 23-26). Hagino discloses a TFT with semiconductor layer having a peak-to-valley height difference of 60 nm with highly reliability (see [0015] and [0031]). Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to implement a TFTs in a first region with a grain size of less than 1 micron and a surface peak to valley height difference of 20 nm or more for high reliability.

Ogawa discloses a thin film transistor with polycrystalline silicon with a grain size of 3-5 microns in the scanning direction and .5 to 2 microns (column 10 lines 3-13) in the microns in the other direction for high mobility (ie performance) ( $300 \text{ cm}^2 / \text{Vs}$ ) (see column 5 lines 10 – 25). The MPEP states in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a *prima facie* case of obviousness exists. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976). Furthermore Shinigawa discloses a high performance TFT with grain sizes larger than 500 nm and roughness (peak-to-valley) less than 5 nm ([0010]). Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to optimize TFTs in a second to have grain sizes of 4 or more microns in length and .5 to 2 microns in width and lower roughness to less than 5 nm to improve transistor mobility/performance.

**Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki 6512247 in view of Takemura 6335555 in view of Ogawa US Patent No. 6479837 and further in view of Shinigawa et al 20030160239.**

**Regarding claim 9,** Suzuki teaches an image display device with an active matrix substrate (see fig. 13) having a plurality of circuit regions fabricated on one insulating substrate and including at least a pixel section and a pixel-driving circuit section, each of said pixel section and said pixel driving-circuit section having TFTs formed of polycrystalline silicon films, wherein said polycrystalline silicon films in a channel source and drain region constituting TFTs of the pixel section have an average crystalline diameter is 1 micron or smaller (see column 2 lines 35-47). Suzuki fails to teach pixel TFTs having a peak-to-valley height difference of 20 nm or greater however Takemura teaches that TFTs found in the pixel region demand high reliability (see column 16 lines 44-51). Hagino discloses a TFT with semiconductor layer having a peak-to-valley height difference of 60 nm with highly reliability (see [0015] and [0031]). Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to incorporate a surface peak to valley height difference into the pixel TFTs of Suzuki to gain high reliability.

Suzuki teaches that a grain size of at least 3 microns in length for peripheral TFTS that demand high performance (see column 5 lines 13-28) however fails to teach any peak-to-valley value or any rectangular shaped grains. Ogawa discloses a thin film transistor with polycrystalline silicon with a grain size of 3-5 microns in the scanning direction and .5 to 2 microns (column 10 lines 3-13) in the microns in the other direction for high mobility (ie performance) ( $300 \text{ cm}^2 / \text{Vs}$ ) (see column 5 lines 10 – 25). The MPEP states in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a *prima facie* case of obviousness exists. *In re Wertheim*, 541

F.2d 257, 191 USPQ 90 (CCPA 1976). Furthermore Shinigawa discloses a high performance (high mobility) TFT with grain sizes larger than 500 nm and roughness (peak-to-valley) less than 5 nm [0010]. Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to further optimize Suzuki's TFTs with grain sizes of 4 or more microns in length and .5 to 2 microns in width and lower roughness to less than 5 nm to improve transistor mobility which is necessary for peripheral (driving circuit) TFTs.

**Regarding claim 11,** the limitation TFTs having “plural kinds of structures” according to the broadest reasonable interpretation can include having a TFT having a source gate and drain electrodes as the plural structures, which is met.

**Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi in view of Kwak 6509940.**

**Regarding claim 7,** Yamauchi teach all the limitations of claim 10 except plural kinds of gate insulating materials. Kwak teaches that it is conventional in the art to use silicon nitride or silicon oxide gate insulation films in polycrystalline silicon TFTs (see ). Conventionality has associative benefits such as known implementations and lower costs. Furthermore an additional gate insulation material provides greater flexibility in design. Therefore, at the time of the invention it would have been obvious to one of ordinary skill to use silicon nitride or silicon oxide gate insulation films to gain greater design flexibility and benefits of conventionality.

**Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Takemura in view of Ogawa in view of Shinagawa and further in view of Kwak 6509940.**

**Regarding claim 10,** Suzuki, Takemura, Ogawa and Shinagawa teach all the limitations of claim 10 except plural kinds of gate insulating materials. Kwak teaches that it is conventional in the art to use silicon nitride or silicon oxide gate insulation films in polycrystalline silicon TFTs (see ). Conventionality has associative benefits such as known implementations and lower costs. Furthermore an additional gate insulation material provides greater flexibility in design. Therefore, at the time of the invention it would have been obvious to one of ordinary skill to use silicon nitride or silicon oxide gate insulation films to gain greater design flexibility and benefits of conventionality.

**Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Takemura in view of Ogawa in view of Shinagawa in view of Kwak and further in view of Zhang US 6249333.**

**Regarding claim 12,** Suzuki, Takemura, Ogawa, Shinagawa and Kwak teach an average crystalline grain diameter of 1micron or smaller and a peak-to-valley height difference of 20 nm or greater in the pixel region (see claim 9 region), however they fail to teach TFTs of a buffer circuit having a polycrystalline silicon film having grains of a rectangular shape of .3 microns to 2 microns in width and 4 or more microns in length and a peak-to-valley height difference of 5 nm or less. The references do teach that it would have been obvious to one of ordinary skill in the art to apply these to all peripheral driving circuits however (see claim 9 rejection). Zhang teaches that

peripheral driver circuits comprise shift register circuits, buffer circuits, and sampling circuits (see column 3 lines 15-18). Therefore, it would have been obvious to one of ordinary skill in the art for transistors of the buffer circuit to have polycrystalline silicon films having grains of a rectangular shape of .3 microns to 2 microns in width and 4 or more microns in length and a peak-to-valley height difference of 5 nm or less as the references taught these have increased mobility, which is a property a property that is suited to high performance driving circuits (see claim 9 rejection)

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

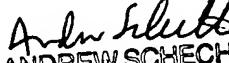
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu Vu whose telephone number is (571)-272-1562. The examiner can normally be reached on 8AM-5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571)-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phu Vu  
Examiner  
AU 2871

  
ANDREW SCHECHTER  
PRIMARY EXAMINER